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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,464	09/08/2003	Masakatsu Uneme	N26532602E	9792

7590 03/06/2007

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/657,464	**Applicant(s)** UNEME, MASAKATSU	
	Examiner Hong C. Kim	**Art Unit** 2185	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 16 February 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: *See Continuation Sheet*. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: *1-8*.
   Claim(s) objected to: *12 and 13*.
   Claim(s) rejected: *9-11 14-20*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☒ Other: Attachement A.

HONG CHONG KIM
PRIMARY EXAMINER

Continuation of 3. NOTE: It appears that added limitation raises new issues that would require further considerationa and search. Applicant's arguments filed 2/16/07 have been fully considered but they are not persuasive.

Continuation of 11. does NOT place the application in condition for allowance because: Applicant's remark that the final rejection is improper is not considered persuasive.
The final rejection sent out on 12/19/06 is proper, because the amendment filed on 10/19/06 included new limitations that would further consideration and search (i.e. see claim 1).
In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Muramatsu discloses subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state (constitution) for the purpose of access to a shared memory in time division.
It appears that an English translation of Muramatsu is not required since the Examiner has rejected claims based on the abstract not the full text, see MPEP 706.02 (II). The examiner includes an English translation of the abstract of Muramatsu with this office action.
Applicant's remarks that the references not teaching data processing circuits is not considered persuasive.
Since a shared memory is accessed at a high level timing, both address and the data buses are at high impedances and the high level timing is provided to each system in alternate fashion Muramatsu discloses wherein when one data processing circuit ends control of the semiconductor memory circuit (abstract and Fig. 2 Ref.9), the data processing circuit provides a control signal at the control output at a predetermined potential for a first time period before ending the control signal; and subsequently, when another data processing circuit (abstract and Fig. 2 Ref. 10) starts control of the semiconductor memory circuit, the data processing circuit provides a control signal at its control output at the predetermined potential within the first time period
Applicant's remarks that the references not teaching at least one control line is directly connected to the control input of the semiconductor memory circuit is not considered persuasive.
Muramatsu discloses the at least one control line is directly (a connection between Fig. 2 Refs. 9 or 10 and Ref. 8) connected to the control input of the semiconductor memory circuit and the control output of each of the plurality of data processing circuits.
Applicant's remarks that the references not teaching subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state is not considered persuasive.
Since a shared memory is accessed at a high level timing, both address and the data buses are at high impedances and the high level timing is provided to each system in alternate fashion Muramatsu discloses subsequently placing the first control outputs in a high impedance state and prior to the first control outputs of the first data processing circuit that is ending control of the semiconductor memory circuit is placed in the high impedance state (See Figs. 2 and 3).

Attachement A

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PAT-NO: JP359183455A

DOCUMENT-IDENTIFIER: JP 59183455 A

TITLE: MULTI-COMPUTER SYSTEM

PUBN-DATE: October 18, 1984

INVENTOR-INFORMATION:
NAME
MURAMATSU, KIKUO

ASSIGNEE-INFORMATION:
NAME **COUNTRY**
MITSUBISHI ELECTRIC CORP **N/A**

APPL-NO: JP58058211

APPL-DATE: March 31, 1983

INT-CL (IPC): G06F015/16

US-CL-CURRENT: 362/540

ABSTRACT:

PURPOSE: To shorten the processing time of a multi-computer system by using two system clocks having a 180° phase shift to each other as the basic clocks of two computer blocks and having synchronization between these blocks to give an access to a shared memory in time division.

CONSTITUTION: A system clock ϕA is supplied to a computer block 9; while a system clock ϕB is supplied to a computer block 10 respectively. The data on an address bus or a data bus are effective only when those clocks ϕA and ϕB are set at high levels. When clocks ϕA and ϕB are set at low levels, the internal processing of the computer is carried out. At the same time, both address and data buses are set at high impedances. Therefore an access can be given to a shared memory 8 from the block 9 when the clock ϕA is set at a high level timing. Then an access is possible to the memory 8 from the block 10 when the clock ϕB is set at a high level timing. Thus the synchronization is obtained between blocks 9 and 10, and an access is possible in time division to the memory 8.